

# P&S Modern SSDs

## Cutting-Edge Research in SSDs

Dr. Jisung Park

Prof. Onur Mutlu

ETH Zürich

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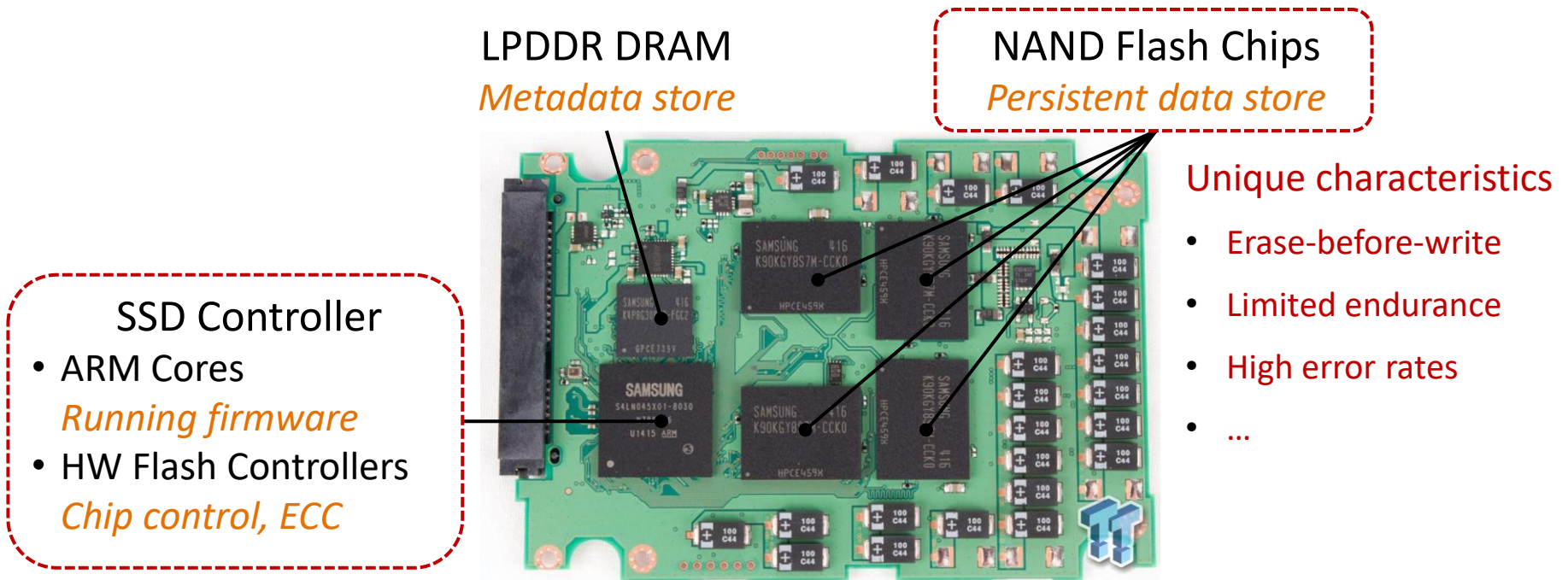
# Outline

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- **NAND Flash Basics**
  - Reducing Solid-State Drive Read Latency by Optimizing Read-Retry, ASPLOS 2021
  - Evanesco: Architectural Support for Efficient Data Sanitization in Modern Flash-Based Storage Systems, ASPLOS 2020
  - DeepSketch: A New Machine Learning-Based Reference Search Technique for Post-Deduplication Delta Compression, FAST 2022
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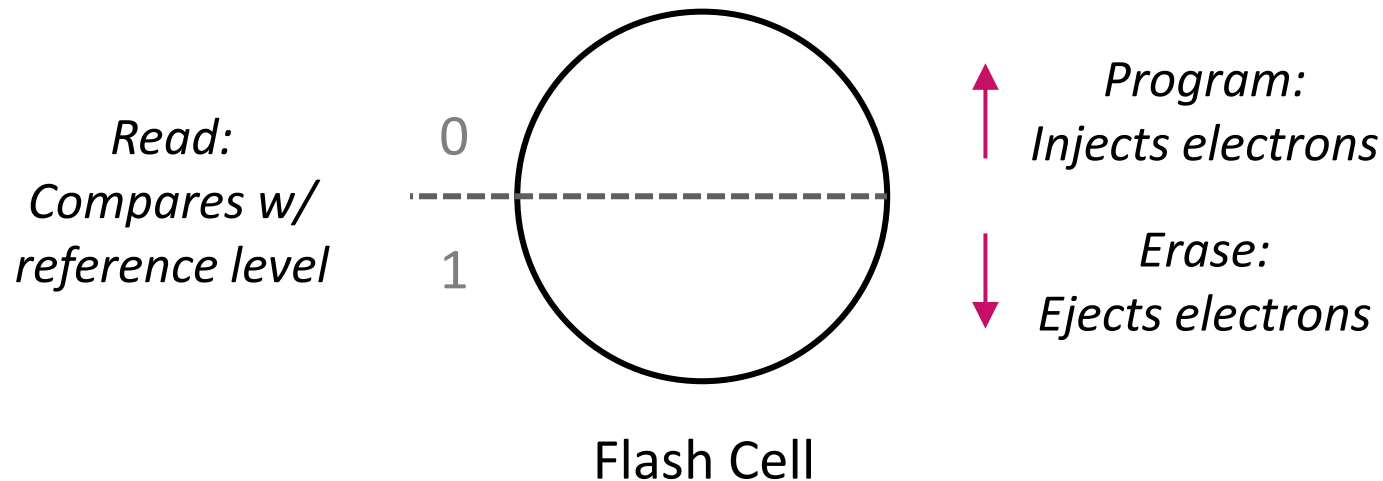
# NAND Flash-Based SSDs

- A complicated embedded system
  - Multiple cores, HW controllers, DRAM, and NAND flash chips



# Flash Cell

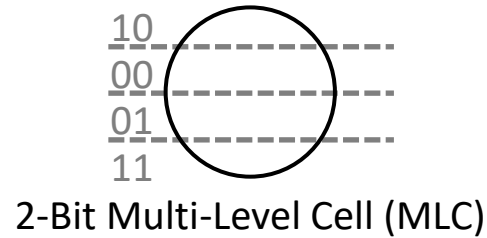
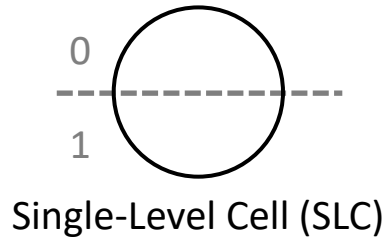
- Stores data using its **threshold voltage ( $V_{TH}$ ) level**
  - Dictated by the **amount of electrons (i.e., charge)** in the cell
  - The more the electrons, the higher the  $V_{TH}$  level



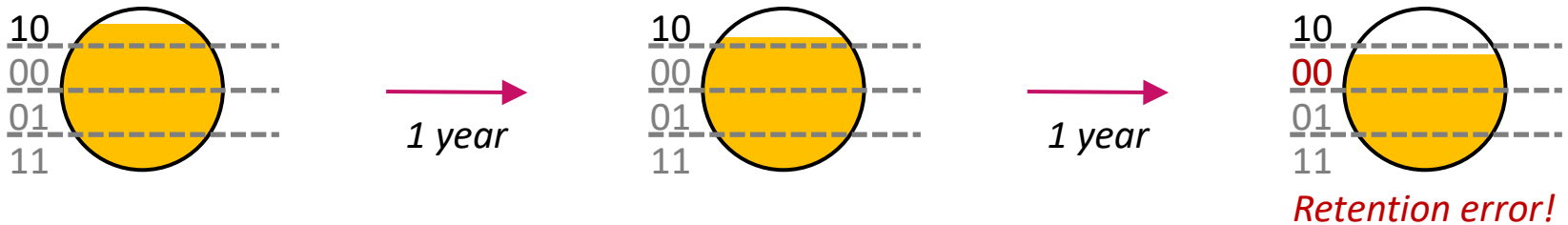
1. Can change  $V_{TH}$  (=charge) in a non-volatile manner
2. Encodes bit data with different  $V_{TH}$  ranges

# Flash Cell Characteristics

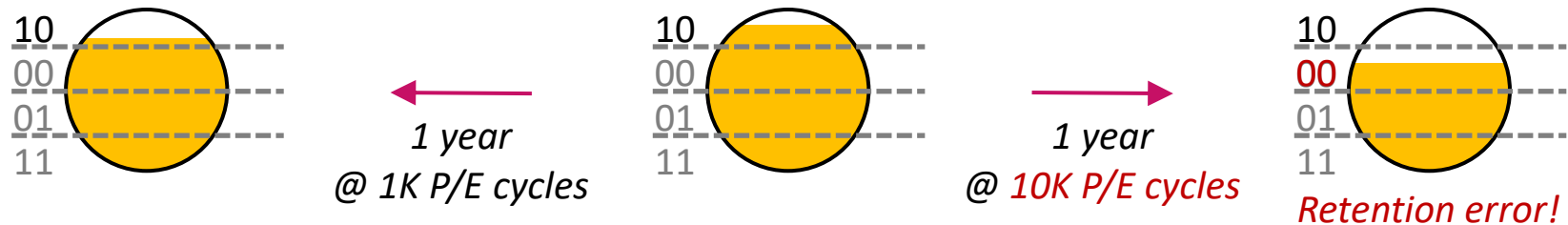
- Multi-leveling: A single flash cell can store multiple bits



- Retention loss: A cell leaks electrons over time



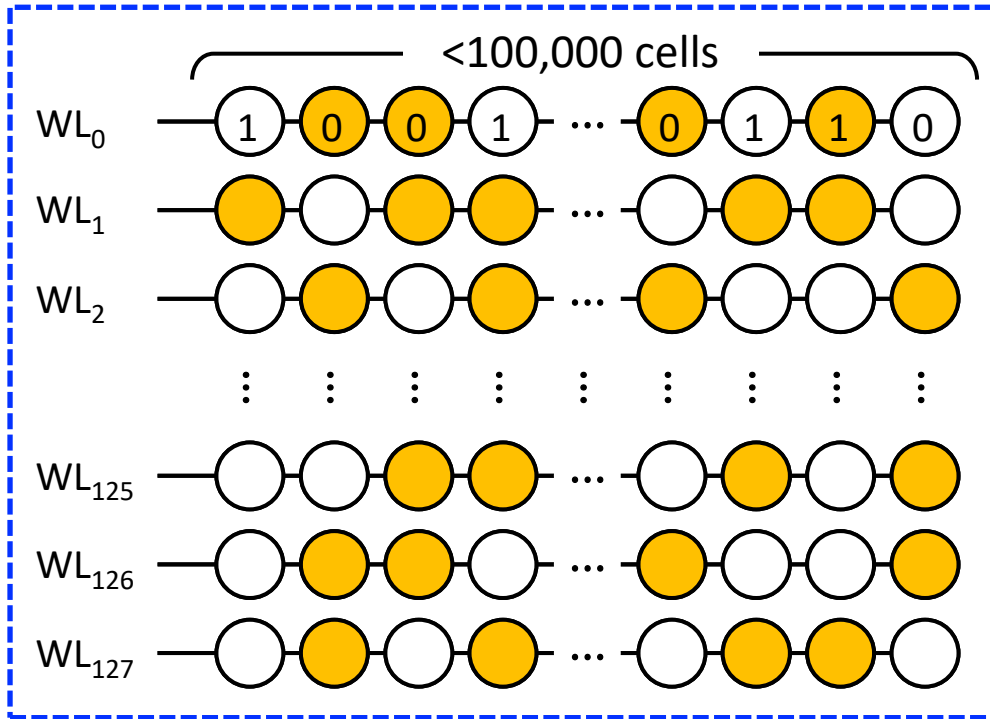
- Limited lifetime: A cell wears out after P/E cycling



# Page and Block

- A number of flash cells operate **in parallel**

Cells in the same wordline (WL)  
are **concurrently read/programmed**



## Block (128 WLs)

Cells in the same block  
are **concurrently erased**

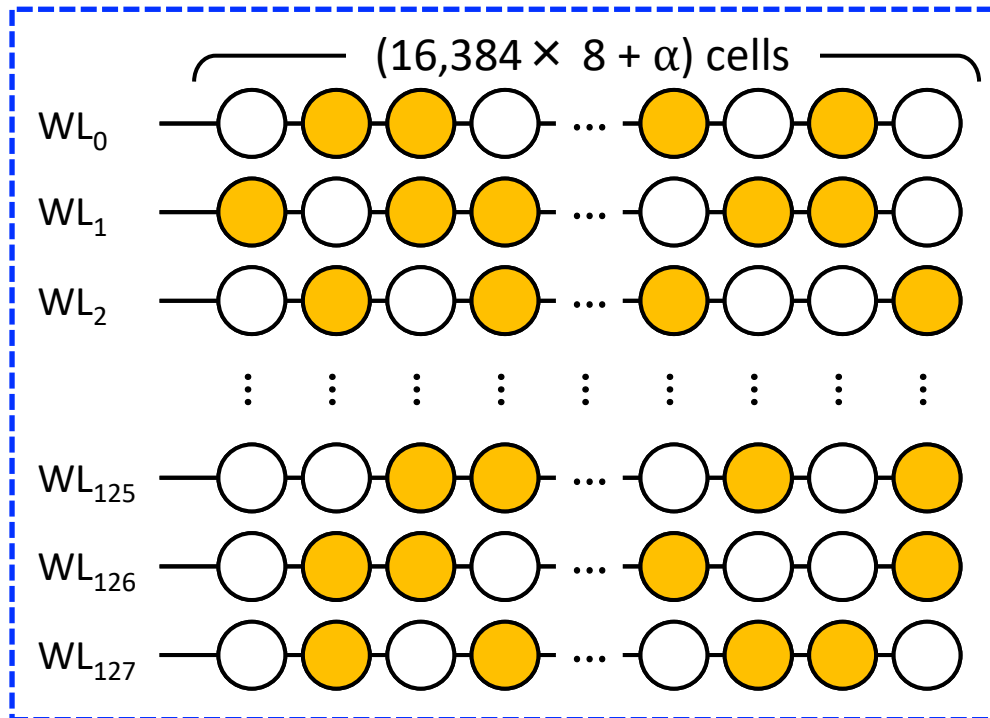
Long latency,  
but high bandwidth

No overwrite of WLs  
before erasing the block:  
*Erase-before-write*

# Page and Block

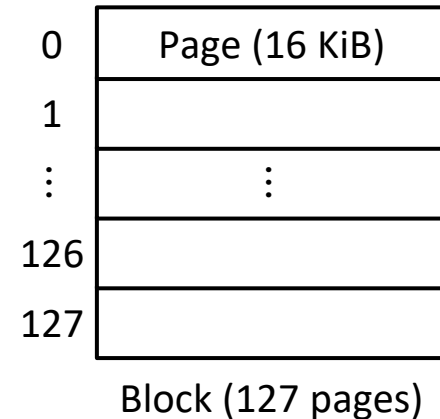
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Block (128 WLs)

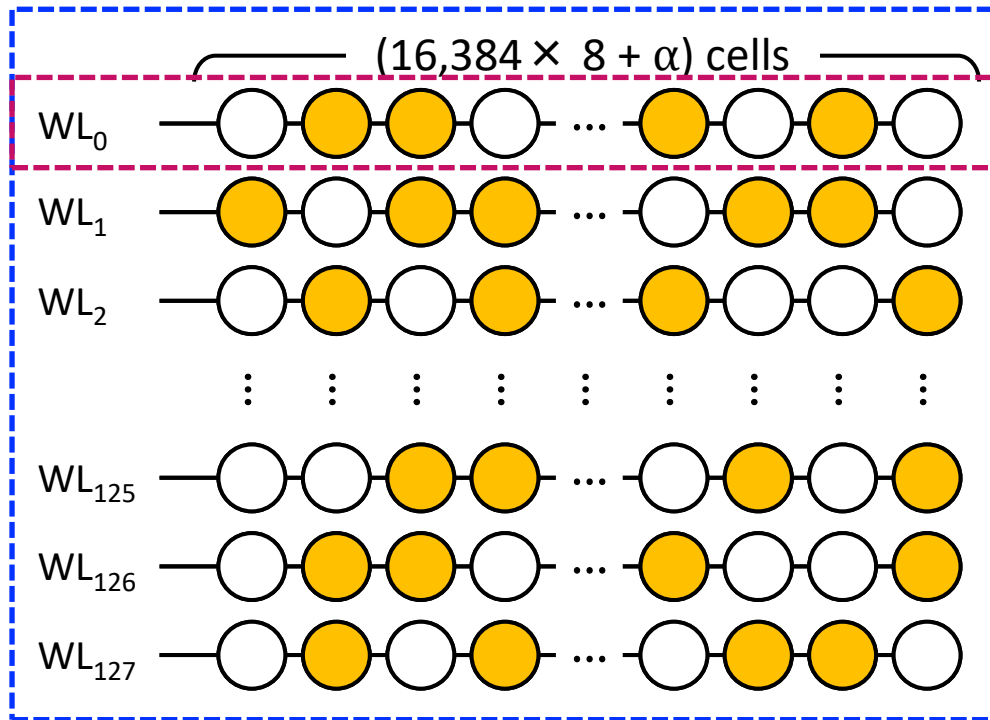
*Cells in the same block  
are **concurrently erased***



# Page and Block

- A number of flash cells operate **in parallel**

Cells in the same wordline (WL)  
are **concurrently read/programmed**



Block (128 WLs)

Cells in the same block  
are **concurrently erased**

Share the same cells (WL)

0	Page (16 KiB)
1	
2	
3	
4	
$\vdots$	$\vdots$
378	
379	
380	
381	

Triple-Level Cell (TLC)  
Block ( $127 \times 3$  pages)



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